Daffodil International University

Faculty of Science & Information Technology

Department of Computer Science & Engineering

Final Examination, Fall 2024

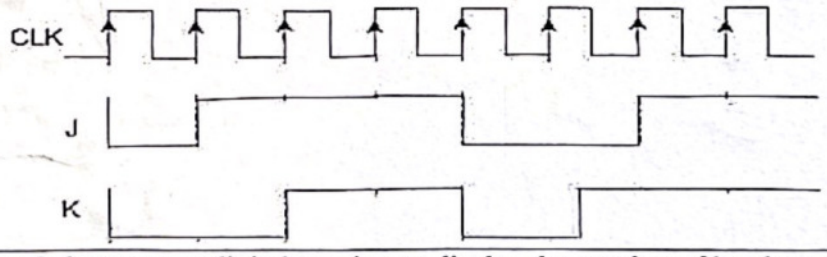
Course Code: CSE223, Course Title: Digital Logic Design

Level: 2 Term: 2 Batch: 64

Time: 02:00 Hrs **Marks: 40**

Answer All Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	a)	A smart home system is designed to automatically control the room light and fan. The system turns on the light and fan based on the conditions below. • At night, if any motion is detected, then the light will switch on. • During the day, if any motion is detected and the sunlight is not sufficient, then the light will switch on. • If the temperature is high and motion is detected, then the fan will switch on. Construct the truth table, derive the Boolean expression, and draw the logic circuit for the above scenario.	[10]	CO3
	b)	Implement 1x16 De-multiplexer using 1x2 De-multiplexer.	[5]	
2.	a)	Explain the difference between synchronous and asynchronous counter circuits. Provide one example of each.	[5]	CO4
3.	a)	Identify the output states Q and Q' for J-K flip flop, given the following pulse inputs.  	[5]	
	b)	A bakery uses a digital monitor to display the number of batches of bread baked during a day. Since the oven can bake up to 10 batches in a shift, it resets after every 10 batches. Thus the monitor displays the batch number (from 0 to 9) for each baking cycle. Now design an appropriate ripple counter using JK flip-flops to display the batch number. Draw the circuit diagram, provide the truth table, and explain how the counter operates.	[10]	
	c)	A vending machine outputs a product when specific conditions are met: • Condition 1: $F1(A,B,C) = \sum(1,3,5)$ • Condition 2: $F2(A,B,C) = \sum(2,6,7)$ Construct the PLA implementation for F1 and F2. Create the truth table, show the required connections, and explain how the PLA realizes the logic.	[5]	