Daffodil International University

Faculty of Science & Information Technology (FSIT)

Department of Software Engineering

Midterm Examination, Summer 2025

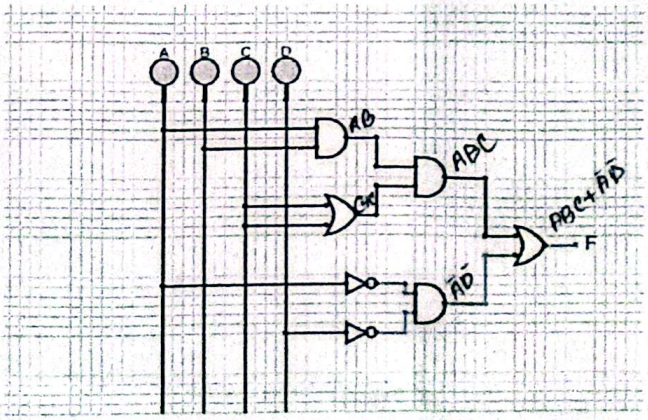
Course Code: SE 213; Course Title: Digital Electronics and Logic Design

Sections & Teachers: SP, HI, MTE, NAN, SAN SHN
Batch and Section: 43 (A to O)

Time: 1 Hour 30 Mins **Marks: 25**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	***a)***	**Subtract** the following using 2's complement: i) $(17)_{10}-(63)_{10}$ ii) $(101100)_2-(1011)_2$	**[Marks-3+2]**	**CLO-1** *Level-2*
	b)	Check the following circuit diagram. **Express** the output logic equation and simplify it: 	**[Marks-5]**	
2.	***a)***	i) **Construct** the Full Adder circuit using basic logic gates. ii) **Apply** Parallel adder to compute (X+ Y) along with diagram: Where X =1 0 1 1 and Y = 1 1 0 0	**[Marks-5+2]**	**CLO-2** *Level-3*
	b)	F (A, B, C, D) = (A+B) (C'+D) +A·C Apply k-map simplification technique to simplify the above expressions. **Construct** the logic diagrams of the simplified output.	**[Marks-8]**	